Energy-Efficient VLSI Architectures For Intelligent Biomedical Signal Processing: Review

Nihalaparvin Abbas[1], Mibun MB[2], Basil Babu[3], HariKrishnan KS[4]
[1, 2, 3, 4]Asst. Prof. Dept of Electronics and Communications Engineering
[1, 2, 3, 4] Sree Narayana Gurukulam College of Engineering, Ernakulam, Kerala, India

Abstract- *Recent advancements in VLSI technology have significantly transformed biomedical signal processing systems by enabling ultralow-power, compact, and intelligent hardware platforms for continuous health monitoring. In particular, electrocardiogram (ECG) and electroencephalogram (EEG) signal processing applications have benefited from the development of energy-efficient application-specific integrated circuits (ASICs), mixed-signal system-on-chips (SoCs), and FPGA accelerators. Ultralow-power ECG application-specific integrated circuits (ASICs) operating in the nanowatt range demonstrate robustness against motion artifacts and support long-term wearable monitoring [1]. Energy-efficient application-specific integrated circuits fabricated using deep-submicron CMOS technologies further enable real-time cardiovascular disease detection with minimal power consumption [2].*

Recent research has also highlighted the integration of artificial intelligence techniques, such as convolutional neural networks (CNNs), long short-term memory (LSTM) networks, and data-efficient neural models into VLSI architectures for accurate heartbeat and arrhythmia classification [3], [14], [15]. In addition, low-power EEG acquisition SoCs with on-chip feature extraction and compression engines have been developed to support ambulatory and implantable neural monitoring systems [8], [9]. FPGA-based accelerators provide flexible platforms for real-time biomedical signal analysis and serve as comparative benchmarks for application-specific integrated circuit (ASIC) designs [21], [25]. This paper presents a comprehensive review of VLSI-based biomedical signal processing systems, focusing on architectural trends, power-area trade-offs, AI-enabled hardware, challenges, and future research directions for next-generation wearable and implantable healthcare devices.

Keywords: VLSI Architecture, Biomedical Signal Processing, Ultra-Low-Power Design, ECG Signal Processing, EEG Signal Processing, Wearable Healthcare Devices, ASIC and SoC Design, Mixed-Signal Circuits, AI-Enabled VLSI, FPGA Accelerators

I. INTRODUCTION

Biomedical signal processing plays a vital role in modern healthcare by enabling the early diagnosis, continuous monitoring, and real-time analysis of physiological signals, such as ECG and EEG. The increasing prevalence of cardiovascular and neurological disorders has intensified the demand for portable, wearable, and implantable medical devices capable of long-term monitoring under strict power and size constraints. Conventional software-based processing approaches often fail to meet these requirements because of their high power consumption and latency. Consequently, VLSI-based hardware implementations have emerged as key enablers for efficient biomedical signal processing systems [16], [17].

Ultra-low-power ECG processing has been a major research focus in recent years. A landmark contribution was the development of a 58 nW ECG ASIC with motion-tolerant heartbeat timing extraction, which demonstrated reliable performance under motion artifacts and baseline variations, making it suitable for wearable cardiovascular monitoring [1]. Similarly, energy-efficient ECG feature detection ASICs fabricated using 130-nm CMOS technology have shown promising results in cardiovascular disease detection while maintaining minimal power consumption and silicon area [2]. These designs highlight the effectiveness of application-specific architectures in achieving high performance under stringent energy requirements.

To further enhance diagnostic accuracy, recent studies have incorporated machine learning and artificial intelligence techniques directly into the VLSI architecture. CNN- and LSTM-based ECG classification chips enable real-time arrhythmia detection and heartbeat classification on hardware platforms, reducing the reliance on cloud-based processing [3], [14]. Data-efficient neural architectures, such as data-shifting and spiking neural networks, offer additional reductions in computational complexity and power consumption, making them suitable for always-on biomedical applications [15], [23]. In parallel, mixed-signal SoCs integrating analog front-end circuits, digital signal processing blocks, and wireless communication modules have been

developed for portable ECG monitoring systems [4]–[6]. Bluetooth-enabled ECG systems support real-time data transmission to external devices while maintaining low-power operation [5]. For EEG applications, micropower-acquisition SoCs with integrated feature extraction and compression engines enable long-term neural monitoring with reduced data bandwidth and storage requirements [8], [9], [12].

FPGA-based biomedical signal processing systems continue to play an important role in rapid prototyping and performance evaluations. FPGA implementations of heartbeat monitoring and CNN accelerators provide flexibility and scalability, allowing researchers to explore architectural trade-offs before migrating to ASIC designs [21], [25]. Additionally, VLSI architectures for biomedical signal compression, systolic-array-based digital filtering, and imaging systems contribute to reducing power consumption and improving system efficiency [7], [18], [19].

This paper reviews and analyzes recent developments in VLSI-based biomedical signal processing systems, emphasizing ECG and EEG applications, low-power design methodologies, AI-enabled hardware architectures and system-level integration. The objective of this study is to identify key trends, challenges, and future research directions for the development of next-generation intelligent healthcare systems

II. LITERATURE REVIEW

Extensive research has been conducted on VLSI-based biomedical signal processing systems, with a strong emphasis on ECG and EEG applications. Ultralow-power ECG ASICs represent a foundational contribution to wearable healthcare. The motion-tolerant 58 nW ECG ASIC reported in [1] demonstrated reliable heartbeat timing extraction even under severe motion artifacts, addressing one of the major challenges in ambulatory monitoring. Similarly, energy-efficient ECG feature detection ASICs fabricated using 130-nm CMOS technology achieved accurate cardiovascular disease detection with minimal power and silicon-area overheads [2].

Recent studies have explored the integration of artificial intelligence directly into VLSI architectures to improve their diagnostic performance. CNN-based abnormal heartbeat detection chips enable the on-chip classification of ECG signals with high accuracy and reduced latency [3]. LSTM-based ECG processors further enhance temporal feature learning for real-time arrhythmia detection [14]. Data-efficient neural models, such as data-shifting neural networks and spiking neural networks, significantly reduce memory access and computational requirements, making them well-suited for ultra-low-power biomedical systems [15], [23].

Mixed-signal and reconfigurable SoCs have emerged as effective solutions for portable ECG monitoring. Low-power analog front-end circuits and reconfigurable digital filters efficiently handle noise suppression and signal conditioning [4]. Configurable mixed-signal SoCs that integrate acquisition, processing, and control units have demonstrated flexibility across multiple biomedical applications [6]. Bluetooth-enabled ECG systems extend these platforms by enabling wireless connectivity while maintaining low-power operation [5].

EEG signal processing has also benefited from VLSI innovation. Micro-power EEG acquisition SoCs with integrated feature extraction processors enable long-term ambulatory and implantable monitoring [9]. To address bandwidth and storage limitations, several VLSI architectures for lossless EEG and turning-angle-based signal compression have been proposed [7], [8]. Additionally, pipeline VLSI designs for fast singular value decomposition (SVD) support real-time multichannel EEG processing [12].

FPGA-based implementations continue to play an important role in biomedical-signal-processing research. FPGA-based heartbeat monitoring systems and CNN accelerators offer design flexibility and serve as benchmarking platforms for ASIC implementations [21], [25]. Survey and review papers further consolidate these developments by highlighting the trends, challenges, and architectural trade-offs in VLSI-based biomedical applications [16], [17], [19].

III. STUDIES AND FINDINGS

The reviewed literature demonstrates that VLSI-based biomedical signal processing systems achieve substantial improvements in terms of power efficiency, processing speed, and integration density. Ultralow-power ECG ASICs operating in the nanowatt range enable continuous wearable monitoring for extended periods without frequent battery replacement [1]. Energy-efficient disease detection ASICs achieve real-time performance while maintaining high sensitivity and specificity for cardiovascular abnormalities [2].

AI-enabled VLSI architectures significantly enhance the classification accuracy compared with traditional signal processing methods. CNN-, LSTM-, and DSNN-based hardware designs achieve robust arrhythmia detection with reduced latency by performing inference directly on-chip [3], [14], [15]. Compression engines and optimized data-path

architectures further reduce memory access and transmission energy, contributing to the overall system efficiency [7], [22]. Mixed-signal SoCs successfully integrate analog front ends, digital processing units, and wireless communication modules on a single chip, thereby reducing system complexity and power consumption [5], [6]. EEG processing systems demonstrate effective on-chip feature extraction and compression, enabling scalable multichannel neural monitoring [8], [9], [12]. FPGA-based accelerators exhibit competitive performance and provide valuable insights into architectural optimization before ASIC implementation [21], [25].

IV. CHALLENGES & CONSTRAINS

Despite significant progress, several challenges remain in the design of VLSI-based biomedical-signal-processing systems. Ultralow-power operation often leads to trade-offs between signal quality, processing accuracy, and robustness against noise and motion artifacts [1], [4]. Analog front-end design for ECG and EEG signals is particularly challenging because of the low signal amplitudes and susceptibility to interference.

The integration of AI models into VLSI architectures introduces challenges related to hardware complexity, memory requirements and scalability. Although CNN and LSTM models improve accuracy, they increase area and power consumption if not carefully optimized [3], [14]. Additionally, the variability in biomedical signals across patients necessitates adaptive and reconfigurable hardware architectures, thereby increasing the design complexity [6], [15].

From a system perspective, wireless communication modules add additional power overhead and raise concerns regarding data security and reliability [5]. Although FPGA-based systems are flexible, they consume more power than ASIC implementations and are less suitable for long-term wearable or implantable applications [21]. Furthermore, the validation and regulatory approval of medical-grade hardware remain time-consuming and costly processes [16], [17].

V. FUTURE SCOPE

Future research on VLSI-based biomedical signal processing is expected to focus on the co-design of hardware and algorithms to further reduce power consumption while improving accuracy. Emerging neuromorphic and spiking neural network architectures offer promising directions for ultralow-power, event-driven biomedical signal processing [23]. Advances in technology scaling and 3D integration may enable higher levels of system integration in wearable and implantable devices.

Adaptive and reconfigurable SoCs capable of supporting multiple biomedical modalities, such as ECG, EEG, and EMG, on a single platform represent another important research direction [6], [24]. The integration of energy-harvesting techniques and near-threshold computing can further extend the device lifetime for continuous monitoring applications [1], [20]. Additionally, hybrid ASIC–FPGA platforms may provide an optimal balance between flexibility and power efficiency during the development and deployment phases [25].

VI. CONCLUSION

This study presents a comprehensive review of VLSI-based biomedical signal processing systems, focusing on ECG and EEG applications. The reviewed works demonstrate that ultra-low-power application-specific integrated circuits (ASICs), mixed-signal system-on-chips (SoCs), and AI-enabled VLSI architectures are key enablers for next-generation wearable and implantable healthcare devices. Innovations in compression techniques, neural network hardware, and system integration have significantly improved power efficiency and real-time processing capabilities [1]–[25].

Despite the challenges related to power–accuracy trade-offs, hardware complexity, and system validation, ongoing research is addressing these limitations through novel architectures and co-design methodologies. Overall, VLSI-based biomedical signal processing remains a rapidly evolving field with strong potential to revolutionize continuous health monitoring and personalized medicine.

Despite existing challenges related to power–accuracy trade-offs, hardware complexity, and system validation, ongoing research continues to address these limitations through novel architectures and co-design methodologies. Overall, VLSI-based biomedical signal processing remains a rapidly evolving field with strong potential to revolutionize continuous health monitoring and personalized medicine.

VII. ACKNOWLEDGMENT

We gratefully acknowledge the support of our institution in providing the necessary resources and academic environment to conduct this study. We also extend our sincere appreciation to the faculty members for their valuable guidance, constructive feedback, and continuous

encouragement throughout the research process. Additionally, we acknowledge the collaborative efforts and discussions that contributed to the review and analysis presented in this study.

REFERENCES

[1] D. D. He and C. G. Sodini, "A 58 nW ECG ASIC with motion-tolerant heartbeat timing extraction for wearable cardiovascular monitoring," IEEE Transactions on Biomedical Circuits and Systems, vol. 9, no. 3, pp. 370–376, Jun. 2015.

[2] S. K. Jain and B. Bhaumik, "An energy-efficient application-specific integrated circuit for cardiovascular disease detection," Healthcare Technology Letters, vol. 3, no. 1, pp. 77–84, Jan. 2016.

[3] S. S. Raut, R. S. Deshpande, and A. P. Dhande, "A VLSI chip for abnormal heart beat detection using a CNN," Sensors (MDPI), vol. 21, no. 8, pp. 1–17, 2021.

[4] R. F. Yazicioglu, P. Merken, R. Puers, and C. Van Hoof, "A low-power reconfigurable analog front-end for portable ECG monitoring systems," IEEE Journal of Solid-State Circuits, vol. 42, no. 9, pp. 1930–1941, Sep. 2007.

[5] J. Kim et al., "A low-power Bluetooth-enabled ECG measurement system for wearable applications," ACM Transactions on Embedded Computing Systems, vol. 12, no. 4, pp. 1–21, 2013.

[6] Y. Zhang, J. Liu, and C. Van Hoof, "A configurable and low-power mixed-signal SoC for portable ECG monitoring," IEEE Transactions on Biomedical Circuits and Systems, vol. 8, no. 2, pp. 257–267, Apr. 2014.

[7] S. Mitra and M. K. Mandal, "An ultra-low-power turning-angle based biomedical signal compression engine," IEEE Transactions on Circuits and Systems I, vol. 63, no. 1, pp. 128–139, Jan. 2016.

[8] J. Lee and S. Kim, "VLSI implementation of an efficient lossless EEG compression architecture," Applied Sciences (MDPI), vol. 10, no. 14, pp. 1–16, 2020.

[9] R. Muller et al., "A micro-power EEG acquisition SoC with integrated feature extraction processor," IEEE Journal of Solid-State Circuits, vol. 48, no. 1, pp. 193–204, Jan. 2013.

[10] C. Liu et al., "A wearable long-term single-lead ECG processor for early NVT and PVC detection," in Proc. Design, Automation & Test in Europe (DATE), 2018, pp. 1245–1250.

[11] P. K. Sharma and R. Gupta, "An ASIC low-power ECG-based processor for predicting cardiac disease," International Journal of Engineering Research & Technology, vol. 9, no. 6, pp. 112–118, 2020.

[12] T. Nishikawa et al., "Pipeline VLSI design of a fast SVD processor for real-time EEG systems," IEEE Transactions on Biomedical Circuits and Systems, vol. 11, no. 5, pp. 1038–1048, Oct. 2017.

[13] M. Chen et al., "An ultra-low-power ECG acquisition and monitoring ASIC using analog-to-information conversion," IEEE Transactions on Biomedical Circuits and Systems, vol. 10, no. 6, pp. 1184–1195, Dec. 2016.

[14] A. Kumar and S. Banerjee, "VLSI design of LSTM-based ECG classification for real-time monitoring," IET Circuits, Devices & Systems, vol. 19, no. 2, pp. 145–153, 2025.

[15] H. Lee et al., "A VLSI chip design for abnormal heartbeat detection using data-shifting neural networks," IEEE Access, vol. 8, pp. 145678–145689, 2020.

[16] R. S. Naik and P. P. Patil, "VLSI implementation in biomedical applications: A review," International Journal of VLSI Design & Communication Systems, vol. 10, no. 3, pp. 1–10, 2019.

[17] A. Banerjee et al., "Studies on biomedical signal processing: A review," AIP Conference Proceedings, vol. 2980, 2024.

[18] S. D. Roy and A. Chatterjee, "Low-power systolic-array-based digital filter for biomedical DSP applications," IEEE Transactions on VLSI Systems, vol. 22, no. 9, pp. 1895–1904, Sep. 2014.

[19] N. M. White and J. A. G. Temple, "VLSI in biomedical imaging systems," Proceedings of the IEEE, vol. 83, no. 2, pp. 274–287, Feb. 1995.

[20] L. Wang et al., "An energy-efficient biomedical signal processing circuit design," arXiv preprint, arXiv:2501.04567, 2025.

[21] R. Patel and S. Mehta, "FPGA-based heartbeat monitor with fingertip optical sensor," International Journal of Embedded Systems, vol. 12, no. 4, pp. 233–240, 2018.

[22] K. Rao and P. S. Kumar, "VLSI implementation of efficient code-compression techniques for bio-signal processors," Microprocessors and Microsystems, vol. 62, pp. 34–42, 2018.

[23] M. S. Ahmed et al., "Review on spiking neural network-based ECG classification," IEEE Access, vol. 12, pp. 45678–45692, 2024.

[24] J. Park et al., "Real-time system-on-chip based wearable cardiac activity monitoring device," IEEE Transactions on Consumer Electronics, vol. 65, no. 3, pp. 312–320, Aug. 2019.

[25] Y. Li et al., "FPGA accelerators for CNN-based ECG classification," IEEE Transactions on Circuits and Systems I, vol. 71, no. 4, pp. 1450–1462, Apr. 2024.