Design of 64-bit Arithmetic Logic Unit (ALU) Based on BSIM4 Model Using Tanner

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Abstract- *Arithmetic circuits play a vital role in computational and digital circuits. Arithmetic Logic Unit (ALU) can perform various arithmetic and logical functions. Proposed 64-bit ALU comprises of different arithmetic functions such as addition, subtraction and logical functions like AND logic, OR logic, NOR logic and NAND logic. ALU always faces the issues of power consumption when there are the complex operations, therefore to overcome this problem the low power 64-bit ALU is designed using adiabatic logic with 180nm CMOS technology. BSIM4 model is used for the implementation of 64-bit full adder, 64-bit AND logic, 64-bit OR logic, 4:1 Multiplexer, 2:1 Multiplexer and Proposed design is verified using tanner EDA (V-13.0) tool. Parametric analysis of 64-bit ALU is done. Proposed Arithmetic Logic Unit is proved to be efficient in terms of Area, Power and Delay.*

Keywords- Arithmetic logic unit, adiabatic logic, CMOS technology, Tanner tool EDA

I. INTRODUCTION

In digital electronics, an arithmetic logic unit (ALU) is a crucial subsystem in digital circuit that performs arithmetic and logical operations. The ALU is a fundamental building block of the central processing unit of a computer. The processors which are found inside modern CPUs provide very powerful and very complex ALUs; a single component may contain a number of ALUs. To achieve the efficiency of the CPU are always determined by the computation efficiency which is based on the ALU design [1]. Arithmetic and Logic unit is one of the major components of the CPU.ALUs of various bit-widths are commonly required in very large-scale integrated circuits (VLSI) from processors to application specific integrated circuits (ASICs) [2]. The ALU is a main block of the central processing unit (CPU) of various digital systems. The designs of these modem digital systems are based on building blocks. System engineers design the architecture of digital systems and determine to connect the devices such as adders, ALU, multipliers, and multiplexers to form digital systems. The advantages of using basic building blocks is to design complex systems include shorter design times, lower cost, higher reliability, higher speeds and more flexibility [3].CMOS technology are assign for a broad range of semiconductor products because of the advantages that CMOS provides: an exceptionally low power-delay product, the ability to accommodate millions of devices on a single chip, and flexible, custom design methodologies which permit optimization, as required, for lowest cost, lowest power, or highest speed. In the recent years, there has been a large progress in the area of computer systems which are produce and based on general purpose micro-processors [4]. ALU is one of the most power hungry building blocks in the processor, increasing the power and thermal issues. The presence of multiple ALUs in current-day processors further creates the problem, impacting the circuit reliability and increasing the power cost. Hence, low power ALU design is highly desirable especially in battery-powered portable applications for extended battery lifespan [7]. At the system-level, reduced power operation is often achieved by scaling the supply voltage VDD downwards, to near-threshold region, and even further to sub-threshold region. Studies have shown that the minimum energy operation of most digital circuits occurs in the sub-threshold region [8].

In this present work the low architecture is designed and simulated. For system layout design, we have used 180nm CMOS technology. Here we have simulated the arithmetic and logic operations. And the parametric analysis of the system, the design steps and obtained results are explained [9]. The design is implemented in such a way that the performance of the system is improved and the power consumption is less. ALU is based on the BSIM4 model which is generally used for the accurate, scalable and predictive MOSFET SPICE model for circuit simulation and CMOS technology development.BSIM4 is the extension of BSIM3.Using the Adiabatic logic the power consumption will be reduced which will help to improve the performance of system, adiabatic logic is a new approach to design the ALU which is originally developed for low power digital circuit.

II. ADIABATIC LOGIC

The term adiabatic logic is given to low-power digital circuit which implements the reversible logic. The term adiabatic comes from the total heat or energy in the system which remains constant. The demand for power-sensitive design has grown significantly in recent years due to

tremendous growth in portable applications. Consequently, the need for power efficient design techniques has grown considerably. Several efficient design techniques have been proposed to reduce the power in VLSI circuit applications. With the scaling of technology and the need for higher performance and more functionality, power consumption is becoming a major bottleneck for microprocessor designs. Adiabatic efficiently reduces the power of the circuit. Adiabatic logic is a form of static CMOS with a couple of fundamental differences with respect to standard CMOS. The main idea is that when the powered-clock is rising, the circuit is evaluated and energy is transported to and stored in the circuit. When the powered-clock is falling, the recovery phase starts, where (most of the) energy is recovered from the circuit by the source. When a circuit capacitance is charged and the supply voltage decreases, the energy stored in the capacitance can be recovered by the source. Otherwise it would have discharged to ground. Only energy stored in capacitances can be recovered, energy dissipated as heat in resistances is lost forever.

2.1 Block diagram for 64-bit ALU

The following diagram shows the input and output signals of ALU to be designed.

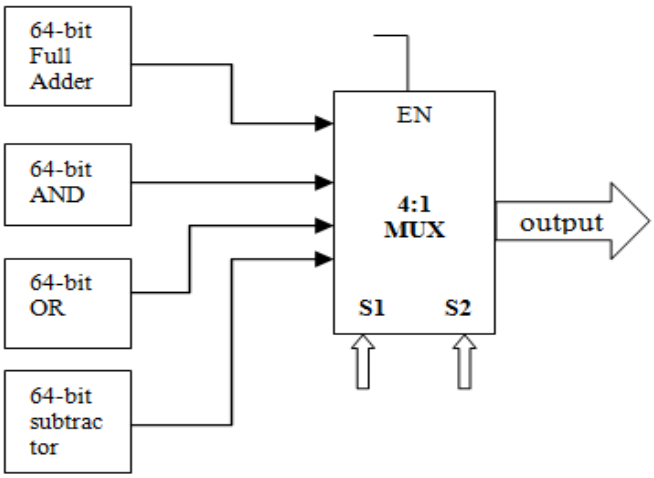

Fig.1 ALU Block Diagram

III. DESIGN APPROACH OF PROPOSED ALU

The proposed ALU circuit is represented by five blocks as shown in fig 1. 64-bit Full adder, 64-bit AND, 64-bit OR, 64-bit subtractor and 4:1MUX. This block is design individually such that the entire circuit is optimized in term of power, delay and area. The section is divided into two parts arithmetic operation and logical operation.

3.1 Arithmetic Operation

The fast and efficient adders in arithmetic operation will aid in the design of low power high performance system. Various adder families have been proposed in the past to trade-off power, area and speed for possible use in ALUs. The performance of the ALU demands a dynamic adder implementation. Dynamic logic family of adders is the most efficient in terms of transistor-count, speed, area, and power dissipation. This work covers by designing the 1-bit full adder and further continuing to 32-bit full adder.

3.1.1 Full Adder Design

In ALU, full adder forms the core of the entire design. The full adder performs the Computing function of the ALU. It consists of three inputs and two outputs. In our design, we have designed the three inputs as A, B and C_{IN}. The third input C_{IN} represents carry input. The outputs are SUM and CARRY. The Boolean expressions for the SUM and CARRY bits are as shown below.

$SUM = A+B+C_{IN}$

$CARRY = A.B+A.C_{IN}+B.C_{IN}$

SUM bit is the XOR function of all three inputs and CARRY bit is the AND function of the three inputs. The symbol for full adder is shown in fig 2.

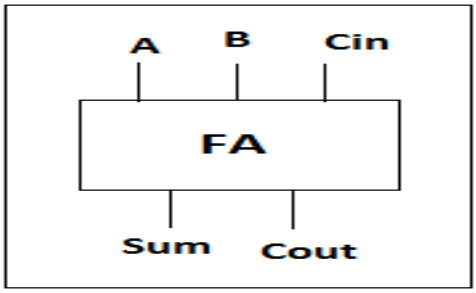

Fig 2.Symbol of Full Adder

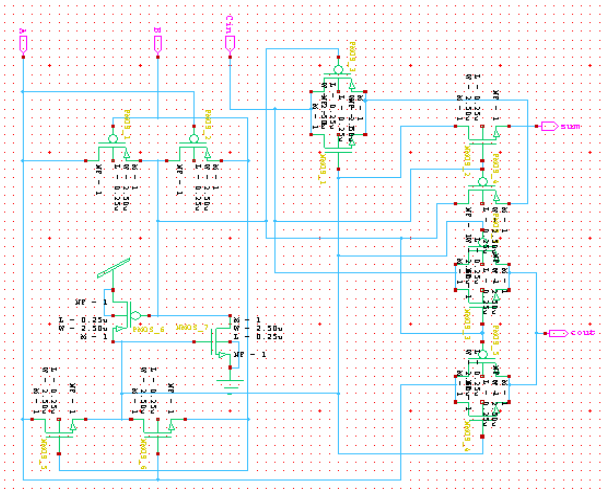

Fig 3.Schematic design of full adder

Output of full adder simulation is as follows

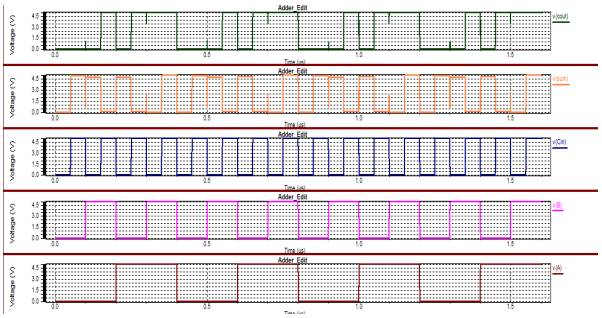

Fig 4.Waveform of full adder

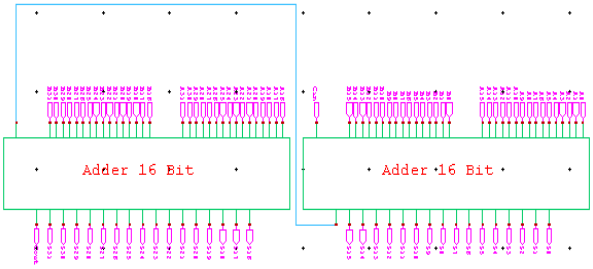

Fig 5.Schematic design of 32-bit Full adder

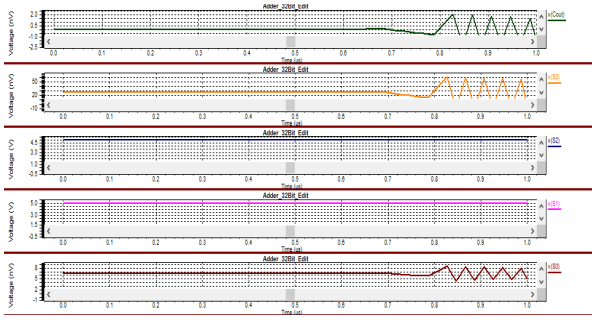

Fig 6.Waveform of 32-bit Full adder

3.1.2 Logical Operation

Logic unit does the following task: AND logic, OR logic, NAND logic, NOT logic. For these operations a special unit is made called as Logical Unit. This Logic Unit asked to perform all logic operations. A MUX is operated by select lines, for which particular logic operation to perform, is used inside this logic block.

A. AND Logic

The fig 3.2 shows the schematic of AND logic. The operations will be performs as shown in following table .Further the design has been extended to 64-bit AND which give the simulation result of 64-bit. The AND gate is a basic gate which can be framed in CMOS by inverting the NAND gate.

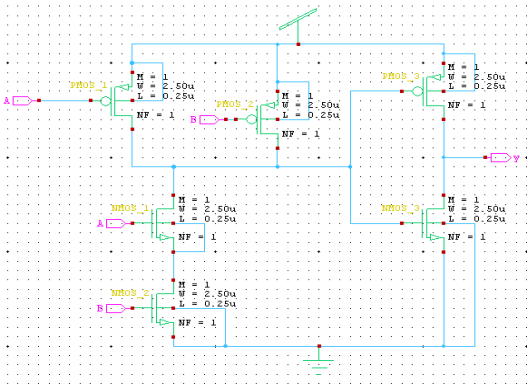

Fig 7.Schematic design of AND Logic

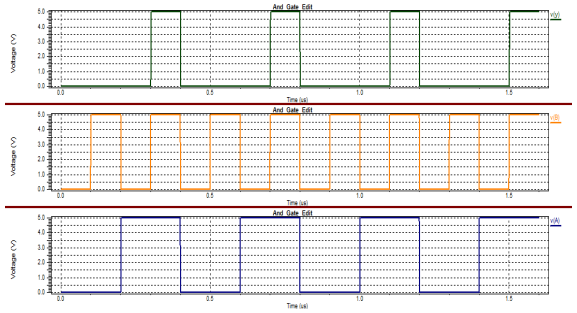

Fig 8.Simlation of AND Logic

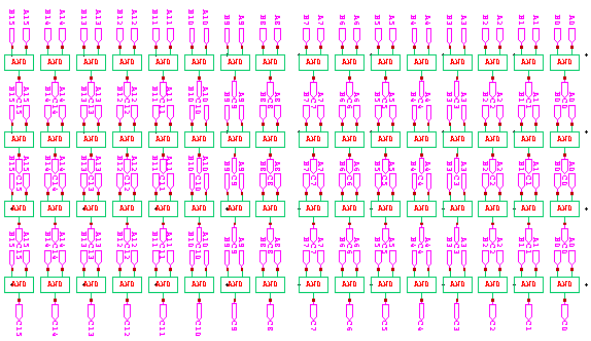

Fig 9.Schematic design of 64-bit AND Logic

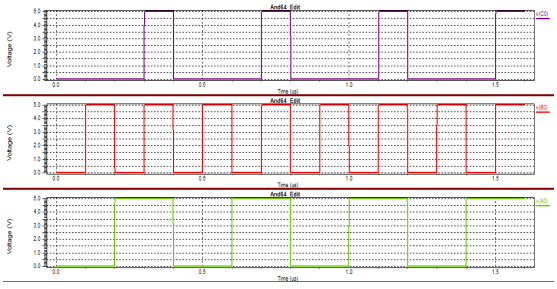

Fig 10.Simulation of 64-bit AND Logic

B. OR Logic

The OR Logic is design in tanner EDA tool using the 180nm CMOS technology. The OR gate is a universal gate and can be constructed in CMOS by inverting the NOR gate. The output of OR is high only when both or any one of the

inputs is high i.e. the output is low only when both the inputs are low.

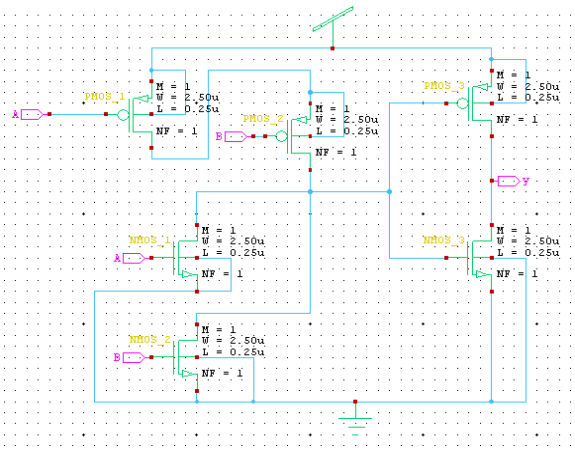

Fig 10. Schematic design of OR Logic

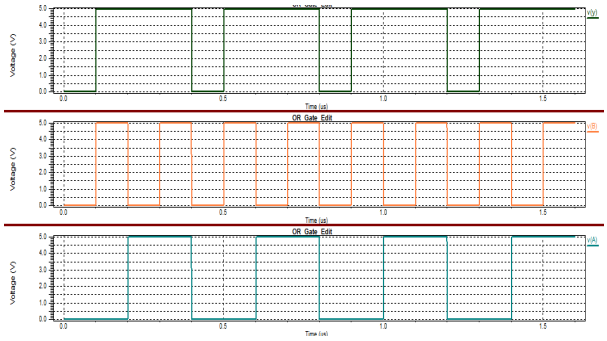

Fig 11.Simulation of OR Logic

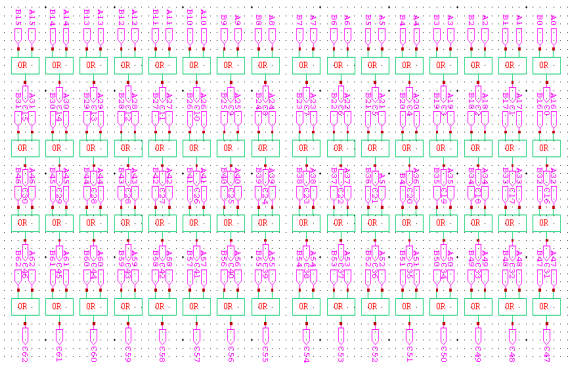

Fig 12. Schematic design of 64-bit OR Logic

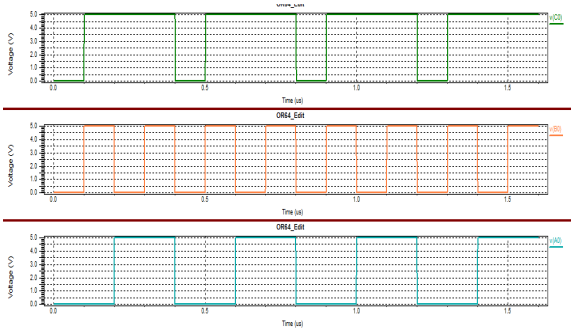

Fig 13.Simulation of 64-bit OR Logic

IV. PERFORMANCE ANALYSIS OF PROPOSED ALU

The simulation of proposed ALU is carried out by using 180nm CMOS technology and compared with the other designs approach of ALU [].

Table 1.Function of ALU

S0	S1	S2	Operation
0	0	0	NONE
0	0	1	AND
0	1	0	NAND
0	1	1	OR
1	0	0	NOR
1	0	1	A+B
1	1	0	A-B
1	1	1	NONE

With the aim to optimize the power of the circuit, the power consumption has been lowered in proposed case. It is observed that in the present design the power consumption is minimized by using the adiabatic logic; which makes the connection from input to output by activating the A and B. The operation performed by the proposed ALU is shown in Table 1.The schematic deigns and simulation of proposed ALU is shown below:

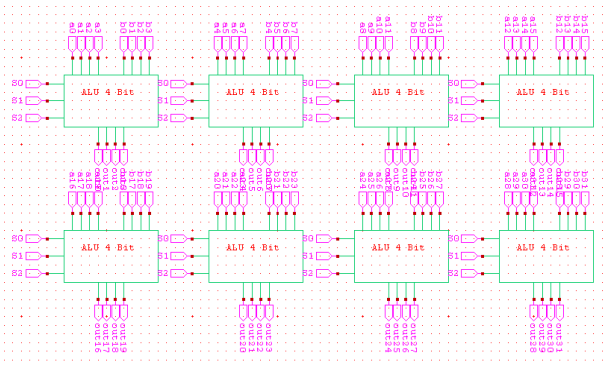

Fig 14. Schematic design of proposed ALU

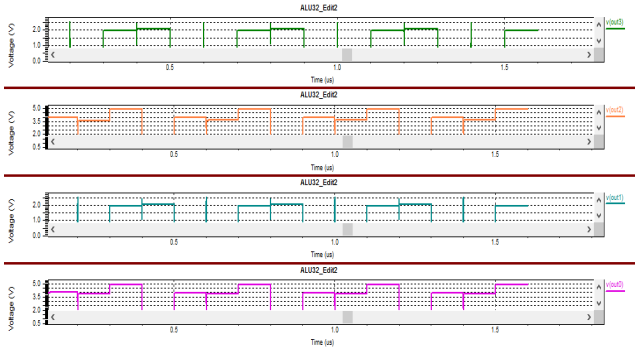

Fig 15.Simulation of proposed ALU

The proposed ALU is design with the help of 4:1 multiplexer and 2:1 multiplexer. It has been used in ALU for the input and output selection. The multiplexers at the input and output select the signals depending on the operation being performed. Transmission gates select one of the inputs based on the value of the control signal. The select signals are S0, S1 and S2. Signal S1 determines if the operation being performed is arithmetic or logical. The multiplexer has a single output, which has the same value as the selected data input. In the present design a 4:1 and 2:1 Multiplexer has been used for each single bit depending on input needed to send out. This also ensures a faster ALU as the functions are performed as soon as the input is fed to the ALU.

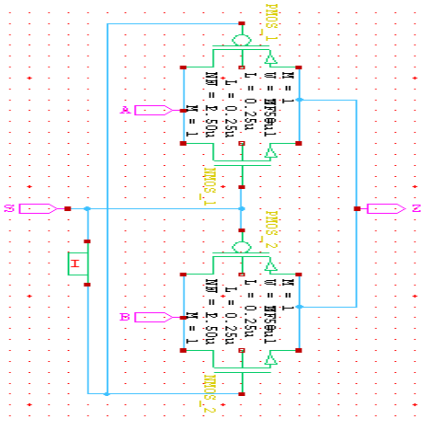

Fig 16.Schematic deign of MUX

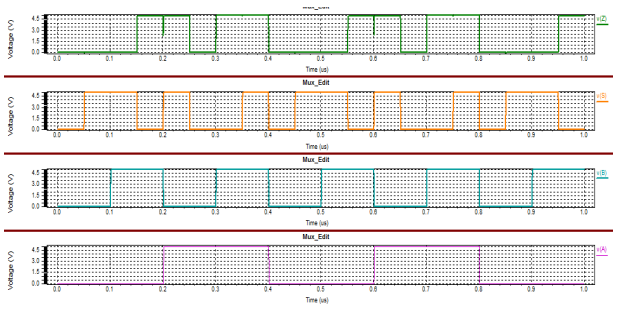

Fig 17.Simulation of MUX

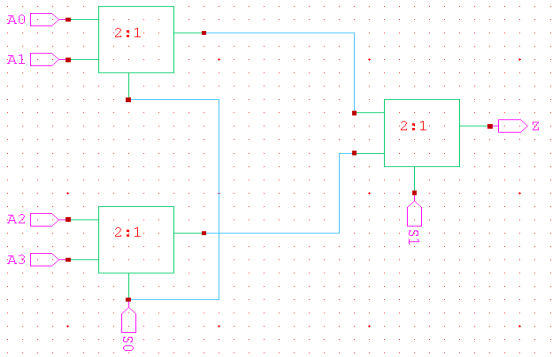

Fig 18. Schematic design of 4:1 Multiplexer using 2:1 MUX

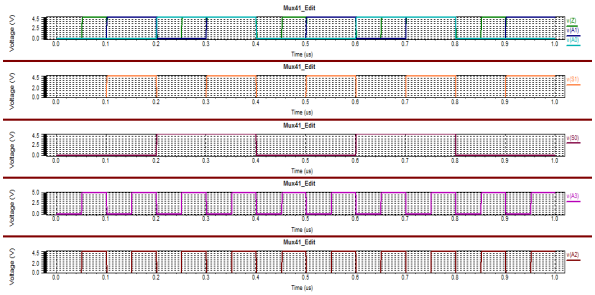

Fig 19.Simulation of 4:1 MUX

V. PARAMETRIC ANALYSIS OF PROPOSED SYSTEM BLOCKS AND COMPARISON OF POWER

The Parameter analysis has been done of each block which has been design in tanner. The following table shows the power, area and delay of AND logic, OR logic, Full Adder and 4:1 MUX.

Table 2 Parameters Analysis of Proposed System

Parameters	Power	Area	Delay
AND	23µw	6	49ms
OR	28µw	6	49ms
Full Adder	17µW	14	SUM=60ms CARRY=49ms
MUX4:1	48µw	18	5ms

The design of ALU is simulated in 180nm technology for comparing the power. The 32-bit ALU is shown to be similar with SLTI and PCBH [1].The power use up by the proposed 32-bit ALU is important to be not high than SLTI and PCBH. Because of decreasing power of the design 32-bit ALU, it is important to become better in comparison with the earlier ALU. The performance of 32-bit ALU worked very frequently as the earlier ALU. The comparison of power is also shown in graphical form with the previous ALU (fig 6), also the comparison shown in tabular form below table:

Table 3 Comparison of Power Consumption

ALU Design	**Proposed 32-bit ALU Using adiabatic logic**	**32-bit ALU using SLTI [5]**	**32-bit ALU using PCHB [5]**
Average Power Consumption (µw)	5.13	7.2	13.8

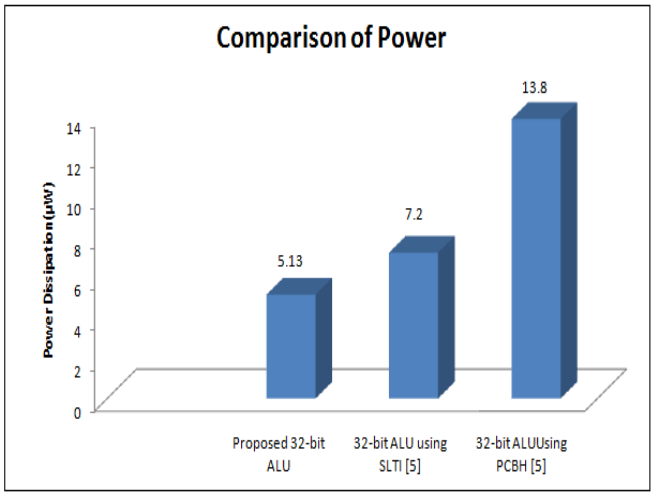

Fig 20. Graphical representation of Power

VI. CONCLUSIONS

An integrated circuit design has been presented for 64-bit arithmetic logic unit using adiabatic logic. The full integrated circuit is designed and simulated in standard 180nm digital CMOS technology. The circuits are simulated in SPICE Tanner EDA tool. Average power for 32-bit ALU by using adiabatic logic, power consumption has been reduce to 5.13µw.The area of 32-bit ALU is 312. Here, using Tanner EDA tool we have designed a 32 bit ALU which can perform the various arithmetic operations of Addition, Subtraction, logical operations such as AND, NAND, OR, NOR and so on. All the above mentioned operations are then verified to see whether they match theoretically or not. The above given waveforms show that they match completely thereby verifying our results.

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